

### **REMARKS**

No claims are amended, no additional claims are canceled, and no claims are added; as a result, claims 1-6, 8-10, 12, 14, 15, 18-23, 31-36, 38-46, and 75-94 are now pending in this application, and wherein claims 15, 18-23, 31-36, 38-46, and 75-93 are withdrawn.

#### **§103 Rejection of the Claims**

##### **Claims 1-6, 8-10, 12, 14 and 94 (Sun/Murata et al.).**

Claims 1-6, 8-10, 12, 14, and 94 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sun (U.S. 6,350,672) and Murata et al. (U.S. 5,268,587). Applicant respectfully traverses this rejection of claims 1-6, 8-10, 12, 14 and 94.

##### **The proposed combination of Sun and Murata et al. fails to teach or suggest all of the elements recited in claims 1-6, 8-10, 12, 14, and 94.**

Applicant submits that each of the elements included in claims 1-6, 8-10, 12, 14, and 94 are not taught or suggested by the proposed combination of Sun and Murata et al. By way of example, but not limited to this example, claim 1 recites,

a conductive structure embedded in a material layer having a plurality of vaporization temperatures, the material layer is formed on the electronic chip and the conductive structure includes a horizontal conductive interconnect and at least one vertical wiring via coupling the horizontal conductive interconnect to the electronic chip,

wherein the horizontal conductive interconnect is formed in and above a fill material.

Thus, claim 1 includes a horizontal conductive interconnect and at least one vertical wiring via coupling the horizontal conductive interconnect to the electronic chip.

In an attempt to supply the horizontal conduct interconnect of claim 1, the Office Action on page 3 states that Sun "includes a horizontal conductive interconnect 78 and at least one vertical wiring via 66 coupling the horizontal conductive interconnect to the electronic substrate." However, and in contrast, Sun at column 8, lines 24-31 states,

In the illustrated embodiments, an intermetal dielectric layer 76 is deposited over the surface of the etch stop layer 72, for example, by CVD of silicon oxide from a TEOS source gas. A via

mask is provided on the intermetal dielectric layer 76, for example, by providing a layer of photoresist which is formed into an etching mask by conventional photolithography. A via is then formed through the intermetal dielectric layer by etching.

And further, Sun at column 9, lines 7-11 states,

After the via is defined through the intermetal dielectric layer 76 extending vertically toward the first level metal wiring line 66, the via etch is continued through the etch stop layer 72 and capping layer 70 to reach the surface of the first level wiring line 66. (Emphasis added).

And further, Sun at column 9, lines 30-32 states,

Processing continues after the via is formed and the surface of the wiring line 66 has been cleared by forming a metal plug 78 to fill the via. (Emphasis added).

Thus, Sun discloses a structure different from that of the conductive structure as recited in claim 1, wherein Sun discloses a metal plug 78 formed in a vertically extending via (as shown in Fig. 9 of Sun) above a first level metal wiring line 66. However, the Office Action fails to show where Sun teaches or suggests a conductive structure embedded in a material layer that includes a horizontal conductive interconnect and at least one vertical wiring via coupling the horizontal conductive interconnect to the electronic chip, as recited in claim 1.

In another example, claim 1 recites, "wherein the horizontal conductive interconnect is formed in and above a fill material." In an attempt to supply these elements, the Office Action on page 3 states, "wherein the horizontal conductive interconnect is formed in and above a fill material 68." (Emphasis added). However, there is no depiction in any of the figures of Sun showing the metal plug 78, (wherein Applicant does not admit that the metal plug 78 of Sun is a horizontal conductive interconnect as recited in claim 1) being in and above a fill material 68. In fact, Sun describes at column 6, line 6 through column 7, line 44, the process of ashing away the carbon layer 68 before the additional layers, such as etch stop material 72 and intermetal dielectric layer 76, are deposited. Thus, there is no disclosure as alleged in the Office Action in Sun of "wherein the horizontal conductive interconnect is formed in and above a fill material," as recited in claim 1. (Emphasis added).

In another example, but not limited to this example, claim 6 recites,

a conductive structure **embedded in a plurality of materials**, each of the plurality of materials having a different vaporization temperature, the plurality of materials is formed on the electronic chip and the conductive structure is coupled to the electronic chip; wherein each **of the plurality of materials contacts a surface of the electronic chip**. (Emphasis added)

In contrast, Sun at column 6, lines 4-16 states,

Next, recesses are preferably formed in the carbon layer 64 by providing the FIG. 6 structure to an ashing or etching system and exposing the carbon layer 64 to an oxygen plasma ashing or etching process. This will produce recessed carbon regions 68 with surfaces spaced from the upper surfaces of first level wiring lines 66 by a few hundred angstroms. The resulting structure is shown in FIG. 7. Next, an oxide layer 70 is deposited over the recessed carbon structures 68 and the first level wiring lines 66 so that the oxide layer extends partially down the sides of each of the first level wiring lines 66.

Thus, Sun discloses an oxide layer 70 deposited over the recessed carbon regions 68 and the first level wiring lines 66. Applicant does not admit that oxide layer 70 or carbon regions 68 are a plurality of materials as recited in claim 6. Further, Applicant submits that there is no disclosure in Sun of a plurality of materials in which the conductive structure is embedded having each of the plurality of materials in contact with a surface of the electronic chip, as recited in claim 6. Instead and in contrast, Sun discloses that both the first level wiring lines 66 and the carbon regions 68 are deposited on interlayer dielectric 62, and thus fails to teach or suggest each the plurality of materials contacting a surface of the electronic chip, as recited in claim 6.

In an attempt to remedy this deficiency, the Office Action on page 4 states,

To further clarify, Sun discloses that each of the plurality of materials contacts a surface of the electronic substrate because the materials and surface are a union of surfaces, and each of the materials is in at least physical association, relationship and connection with a surface of the electronic substrate.

The meaning of "materials and surface are a union of surfaces," and "each of the materials is in at least physical association, relationship and connection" is unclear and

ambiguous. Thus, Applicant submits that the exact meaning of these statements is also unclear and ambiguous. Further, the Office Action fails to point out where these statements are taught or suggested by Sun. Regardless, Applicant submits that Sun fails to teach or suggest wherein each of the plurality of materials contacts a surface of the electronic chip, as recited in claim 6. Thus, Sun fails to teach or suggest each of the elements recited in claim 6.

In a further example of elements not taught or suggested by the proposed combination of Sun and Murata et al., claim 10 recites,

a conductive structure embedded in a material layer having a structural component having a structural vaporization temperature and a fill material having a vaporization temperature less than the structural vaporization temperature, the material layer is formed on the electronic chip and the conductive structure is coupled to the electronic chip,

wherein the conductive structure includes a horizontal conductive interconnect formed in and above the fill material and at least one vertical wiring via coupling the horizontal conductive interconnect to the electronic chip.

For reasons analogous to those stated above with respect to claims 1 and 6, and additional elements included in claim 10, Sun fails to teach or suggest each of the elements recited in claim 10.

Applicant's representatives fail to find in, and the Office Action fails to point out where Murata et al. teaches or suggests these elements included in claims 1, 6, and 10 and missing from Sun. Thus, the proposed combination of Sun and Murata et al. fails to teach or suggest each of the elements included in claims 1, 6, and 10, and so the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1, 6, and 10.

Claims 2-5, 8-9, 12, 14, and 94 depend from one of claims 1, 6, and 10, and therefore include all of the elements recited in the claim from which they depend. Thus, the Office Action also fails to state a *prima facie* case of obviousness with respect to claims 2-5, 8-9, 12, 14, and 94.

The Office Action fails to state a proper basis for forming the proposed combination of Sun with Murata et al.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of

obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

Applicant respectfully maintains each of Applicant's arguments submitted in a previous response to the same proposed combination Sun and Murata et al. In Applicant's previous response mailed September 12, 2005 in response to a prior Final Office Action mailed July 11, 2005 in this same application, Applicant submitted the following:

The Office Action fails to provide proper motivation or suggestion to combine Sun with Murata et al. The Office Action, on page 9 states, "Moreover, it would have been obvious to combine this disclosure of Murata with the disclosure of Sun because it would enable manufacture of a DRAM and reduce the migration phenomenon in the aluminum conductive structure of Sun," and further, on page 10, "it would have been obvious to combine this disclosure of Murata with the disclosure of Sun because it would facilitate provision of the silicon oxide of Sun." Applicant disagrees with these statements. Sun does not appear to concern "manufacture of a DRAM" or "reduction of the migration phenomenon in aluminum conductive structure" or "provision of the silicon oxide," and so the statements in the Office Action are merely conclusory statements based on impermissible hindsight. Because these statements fail to meet the standards as set forth above, the Office Action has failed to state a *prim facie* case of obviousness with respect to claims 1-6, 8-10, 12, and 14.

The Office Action on page 15 states, "This argument is respectfully deemed unpersuasive and traversed because Sun is not relied on in the rejection for a disclosure of manufacturing a DRAM or reduction of migration phenomenon in aluminum conductive structure." While Applicant does not necessarily agree or disagree with this statement, the Office Action does rely on this statement in an attempt to provide a

motivation for combining the references of Sun and Murata et al. Because this statement is not supported by the disclosure of Sun, the Office Action fails to meet the requirements for providing proper motivation or suggestion to combine Sun with Murata et al. regardless of whether or not these statements were relied on to disclose elements recited in the claims. Thus, Applicant maintains that the Office Action fails to state a *prima facie* case of obviousness with regards to claims 1-6, 8-10, 12, 14, and 94 because the Office Action fails to state a proper basis for forming the proposed combination of Sun and Murata et al.

Applicant respectfully maintains each of these above quoted arguments.

In addition, the current Office Action on page 6 states,

Furthermore, it would have been obvious to combine this disclosure of Murata with the disclosure of Sun because it would facilitate provision of the silicon oxide of Sun.

Applicant submits that this statement merely recites what the Office Action proposes would be provided by Sun if the proposed combination of Sun and Murata et al. could be formed (wherein Applicant does not admit that the proposed combination could be formed). However, these statements fail to provide any disclosure in Sun or Murata et al. that would have suggested to those of ordinary skill in the art the forming of the proposed combination of Sun with Murata et al. Further, the statements quoted from the Office Action fail to including some suggestion or incentive to form the proposed combination, as required by the above quoted case law.

Thus, the Office Action is merely forming the proposed combination of Sun and Murata et al. without some suggestion or incentive to do so in an impermissible attempt to reconstruct the claimed invention as recited in claims 1-6, 8-10, 12, 14, and 94. Because the Office Action has failed to provide a proper motivation or suggestion to combine Sun with Murata et al., the Office Action fails to meet the requirements for forming the proposed combination, and so the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1-6, 8-10, 12, 14, and 94 in view of the 35 U.S.C. 103(a) rejection based on the proposed combination of Sun and Murata et al.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 1-6, 8-10, 12, 14, and 94.

Claims 1-4, 6, 10, and 94 (Sun/Wu et al.).

Claims 1-4, 6, 10, and 94 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sun and Wu et al. (U.S. 5,191,404). Applicant respectfully traverses this rejection of claims 1-4, 6, 10, and 94.

The proposed combination of Sun and Wu et al. fails to teach or suggest all of the elements recited in claims 1-4, 6, 10, and 94.

Applicant believes they have established that for at least the reasons argued above, Sun fails to teach or suggest each of the elements included in claims 1-4, 6, 10, and 94. Further, Applicant's representatives fail to find in, and the Office Action fails to point out where Wu et al. teaches or suggests these elements included in claims 1-4, 6, 10, and 94, and missing from Sun. Since the proposed combination of Sun and Wu et al. fails to teach or suggest all of the elements included in claims 1-4, 6, 10, and 94, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1-4, 6, 10, and 94.

The Office Action fails to state a proper basis for forming the proposed combination of Sun with Wu et al.

The Office Action on page 6, in an attempt to meet the requirements for forming the proposed combination of Sun and Wu et al. states,

Furthermore, it would have been obvious to combine this disclosure of Wu with the disclosure of Sun because it would facilitate provision of the electronic substrate of Sun, and enable manufacture of a DRAM and enable external electrical connection of the electronic substrate of Sun.

While Applicant does not necessarily agree with these statements, these statements fail to meet the requirements necessary for forming the proposed combination of Sun and Wu et al., as dictated by the above quoted case law. The Office Action fails to point out how these general statements made on page 6 of the Office Action are supported by the disclosures of either Sun or Wu et al. For example, the Office Action fails to point out any portion of the discourse in Sun concerning "external electrical connection of the electronic substrate."

Further, the Office Action fails to show how these general statements demonstrate some suggestion or incentive for one of ordinary skill in the art to make the proposed combination. Without this, the Office Action is merely forming the proposed combination of Sun and Wu et al. without some suggestion or incentive to do so, in an attempt to produce the claimed invention. However, by failing to meet the requirements as recited above and as quoted from the case law, the Office Action fails to state a *prima facie* case obviousness with respect to claims 1-4, 6, 10, and 94

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 1-4, 6, 10, and 94.

Claim 94 (Sun/Murata et al./Wu et al.).

Claim 94 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sun and Murata et al. as applied to claim 94 supra, and further in combination with Wu et al. Applicant respectfully traverses this rejection of claim 94.

The proposed combination of Sun, Murata et al., and Wu et al. fails to teach or suggest all of the elements recited in claim 94.

Applicant believes they have established that for at least the reasons argued above, the proposed combination of Sun and Matura et al. fails to teach or suggest each of the elements included in claim 94. Further, Applicant's representatives fail to find in, and the Office Action fails to point out where Wu et al. teaches or suggests these elements included in claim 94 and missing from Sun and Murata et al. Since the proposed combination of Sun, Murata et al., and Wu et al. fails to teach or suggest all of the elements included in claim 94, the Office Action fails to state a *prima facie* case of obviousness with respect to claim 94.

The Office Action fails to state a proper basis for forming the proposed combination of Sun, Murata et al., and Wu et al.

The Office Action on page 8, in an attempt to meet the requirements for forming the proposed combination of Sun, Murata et al., and Wu et al. states,



Moreover, it would have been obvious to combine this disclosure of Wu with the disclosure of Sun and Murata because it would enable external electrical connection of the chip of Sun and Murata.

The Office Action fails to point out how these general statements made on page 8 of the Office Action are supported by the disclosures of either Sun, Murata et al., or Wu et al. For example, the Office Action fails to point out any portion of the disclosure in Sun concerning "external electrical connection of the chip of Sun."

Further, the Office Action fails to show how these general statements demonstrate some suggestion or incentive for one of ordinary skill in the art to make the proposed combination. Without this, the Office Action is merely forming the proposed combination of Sun, Murata et al., and Wu et al. absent some suggestion or incentive to do so in an attempt to produce the claimed invention. However, by failing to meet the requirements as recited above and as quoted from the case law, the Office Action fails to state a *prima facie* case obviousness with respect to claim 94.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claim 94.

#### Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

**CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

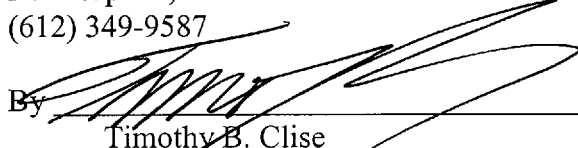
Respectfully submitted,

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Date 24 April '06

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**CERTIFICATE UNDER 37 CFR § 1.8:** The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24 day of April 2006.

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